

FIG. 1

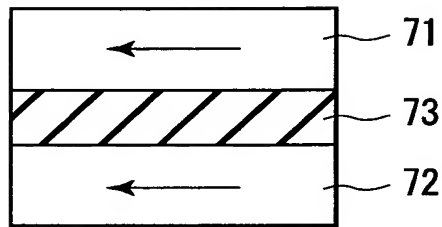
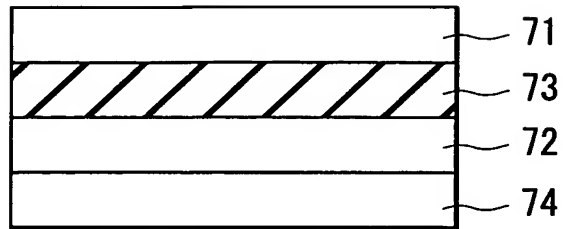


FIG. 2A

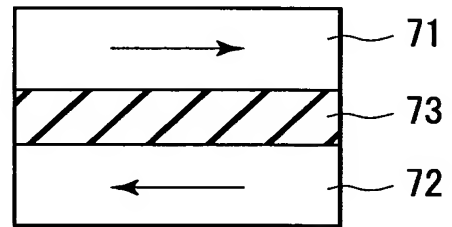


FIG. 2B

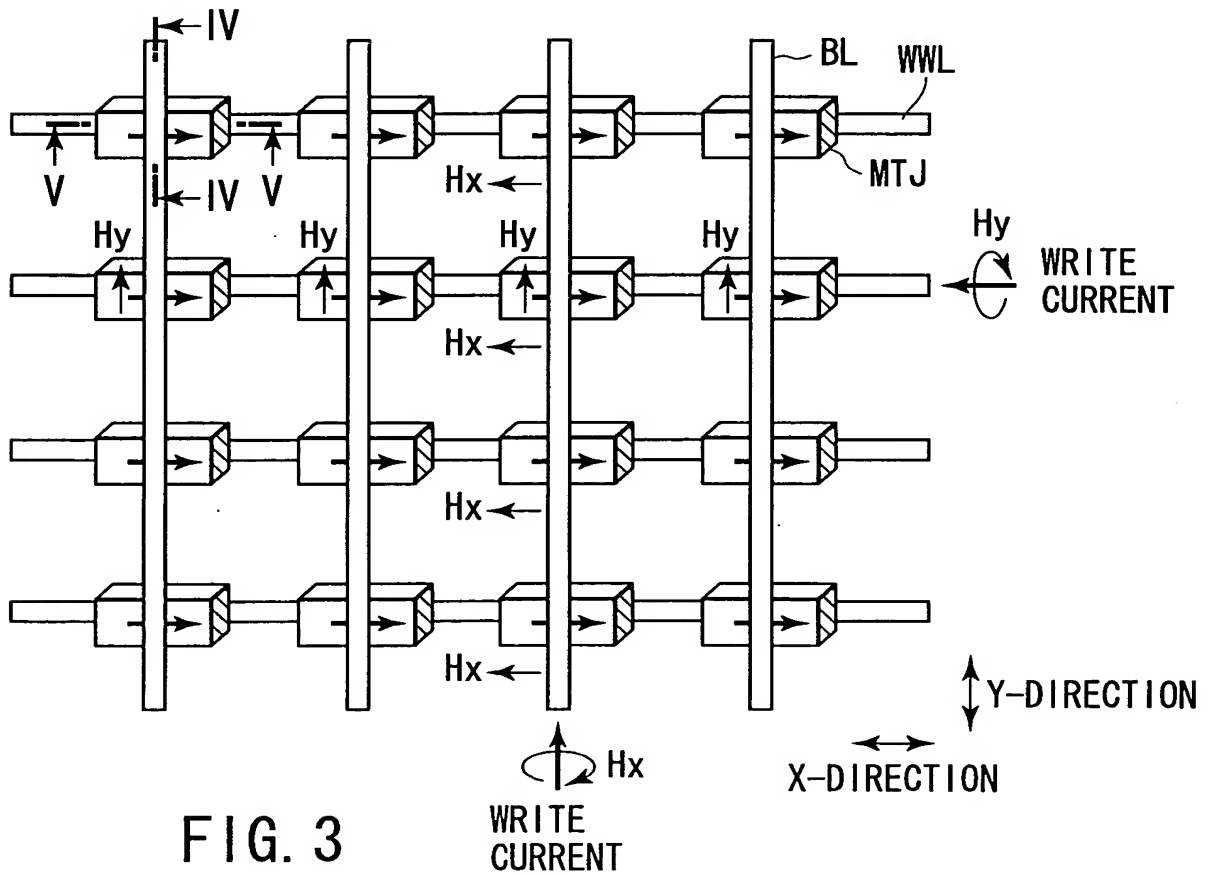


FIG. 3

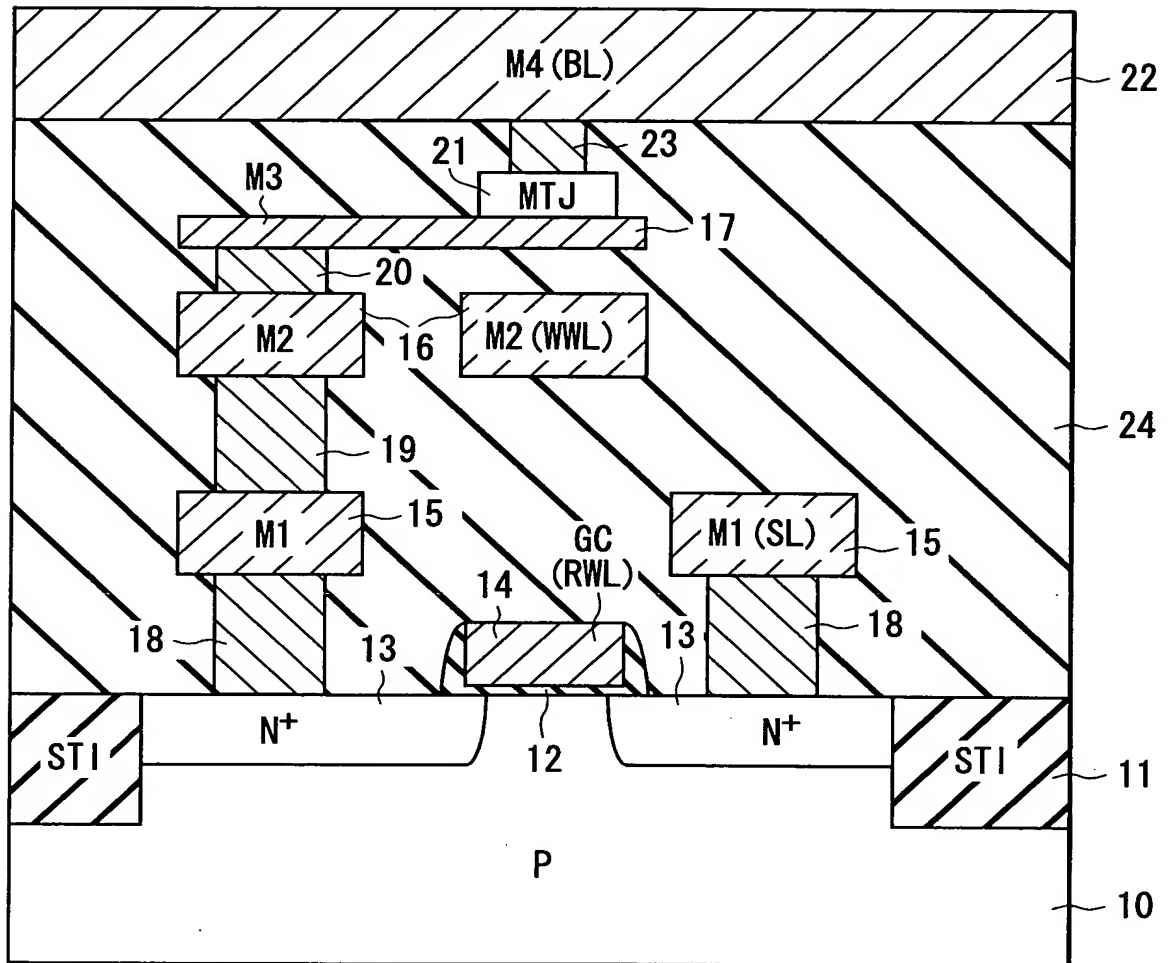


FIG. 4

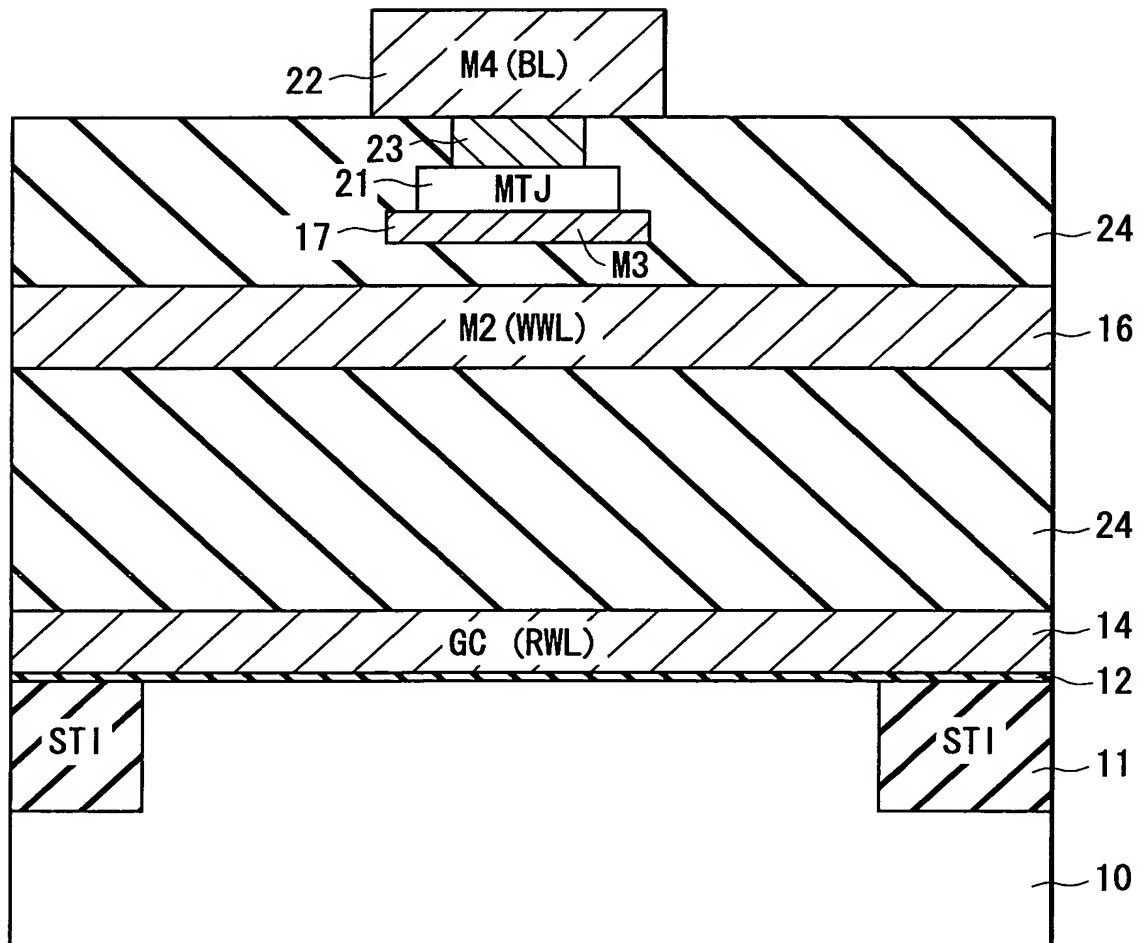


FIG. 5

FIG. 6

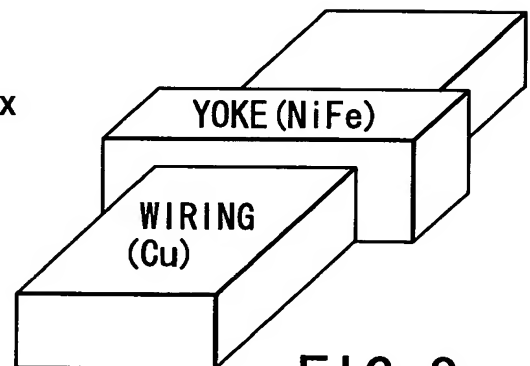
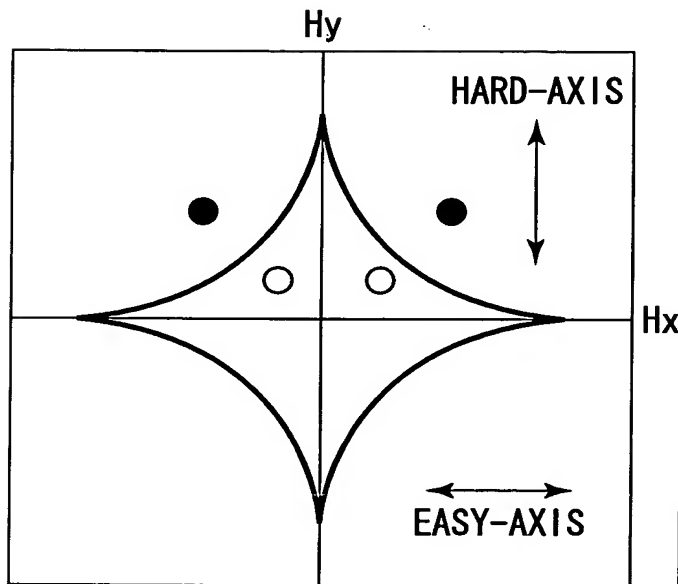
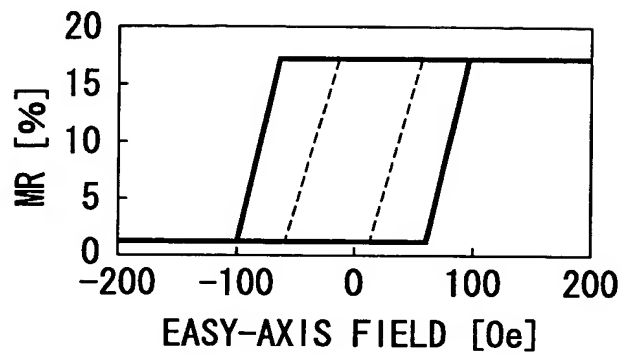


FIG. 8

FIG. 7

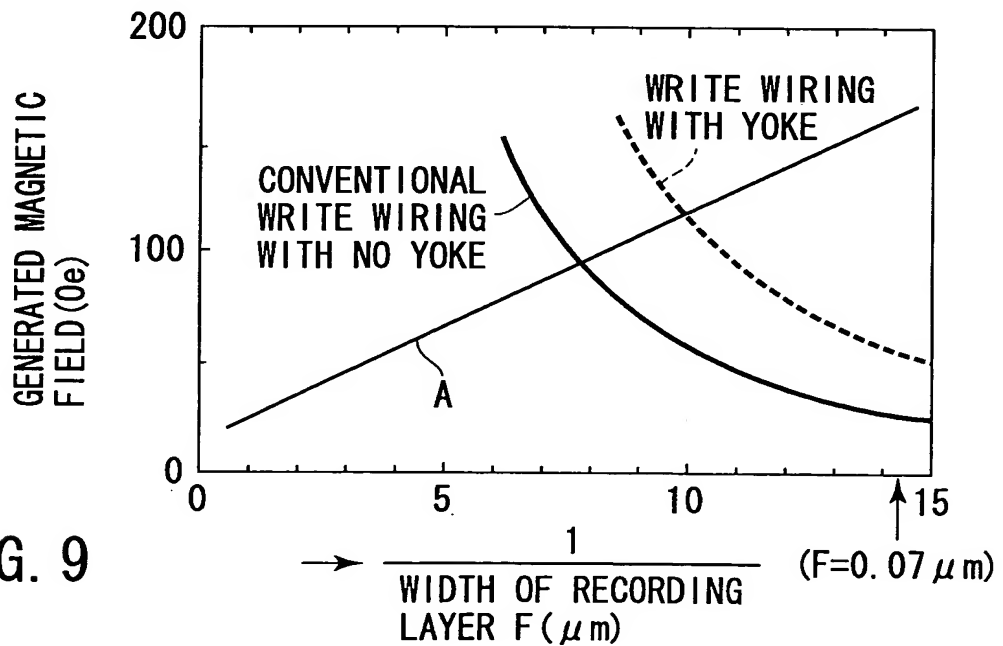


FIG. 9

FIG. 10

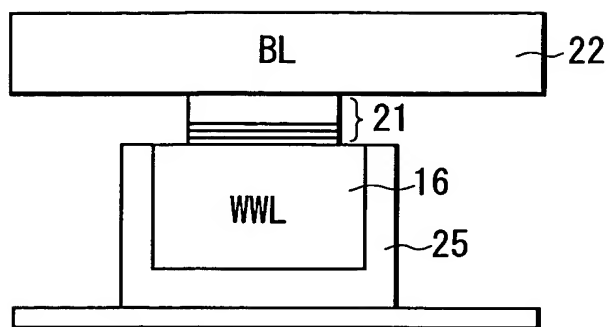


FIG. 11

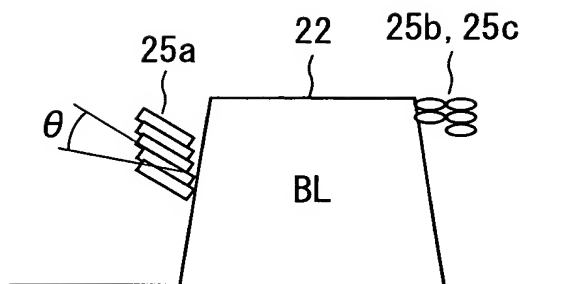
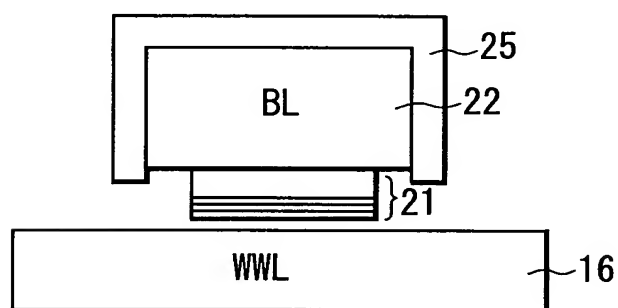


FIG. 12

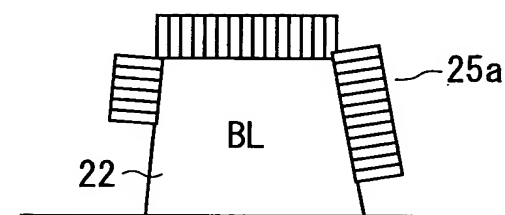


FIG. 13A

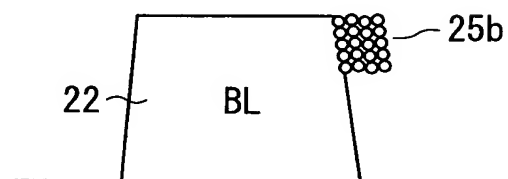


FIG. 13B

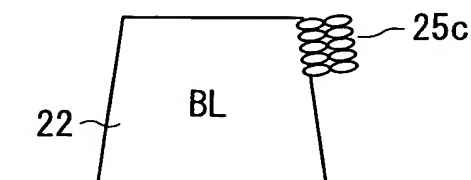


FIG. 13C

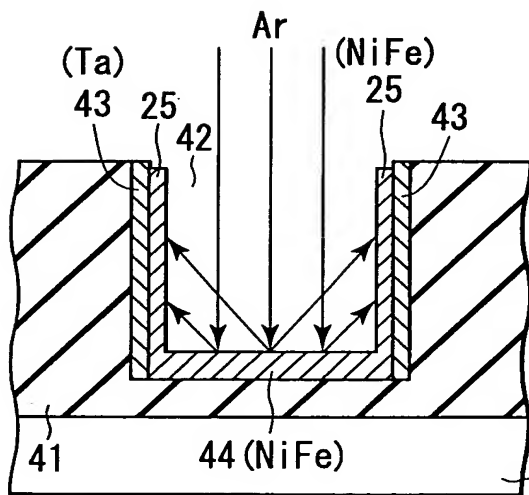
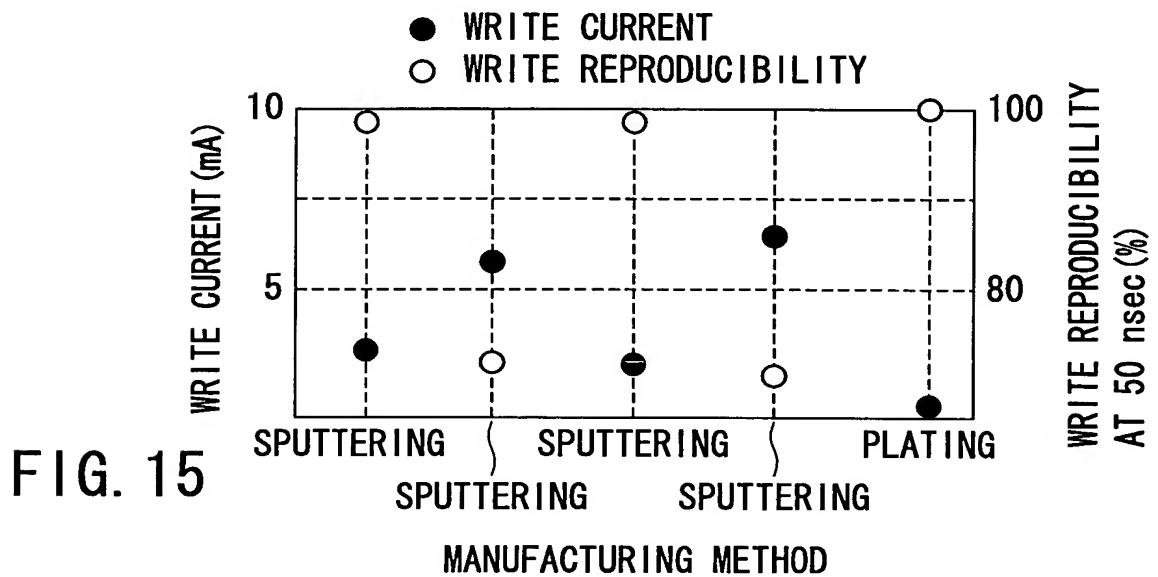
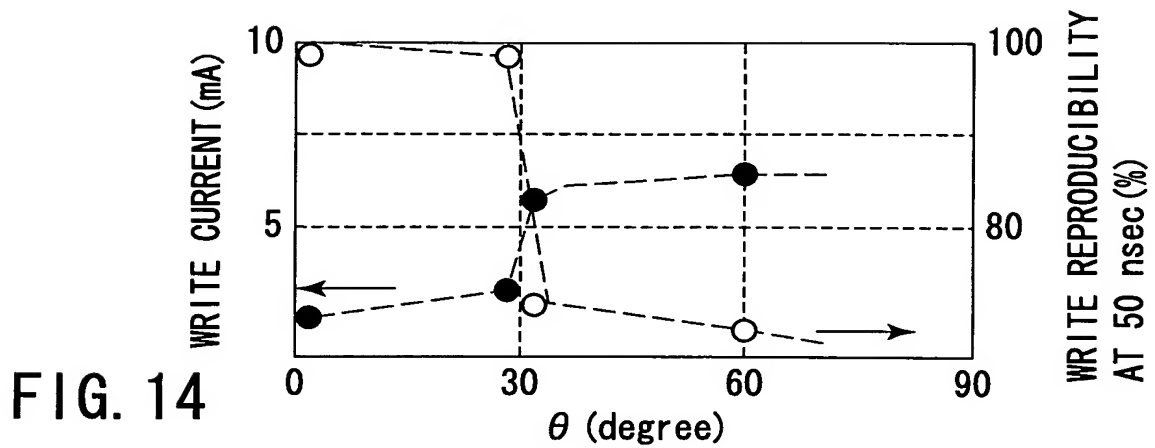


FIG. 16

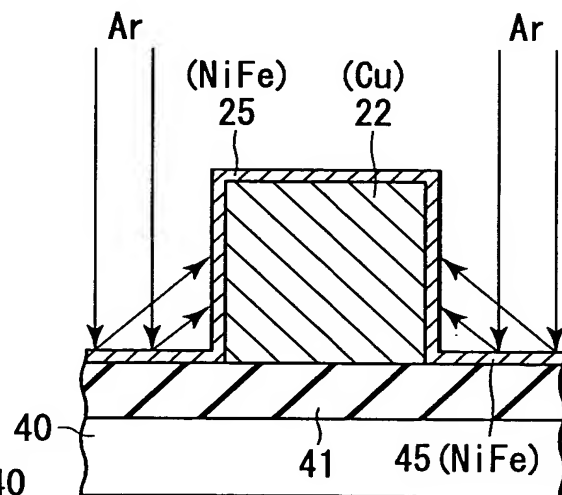


FIG. 17

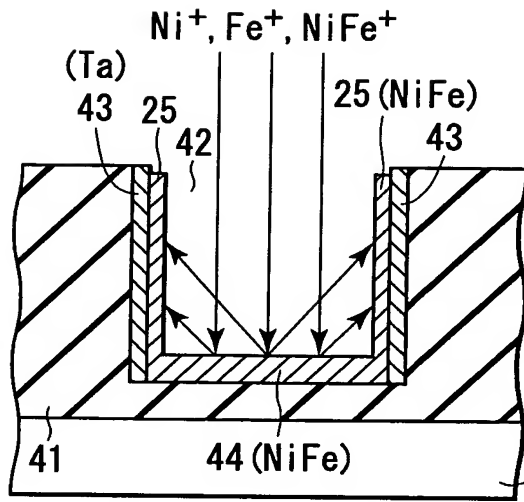


FIG. 18

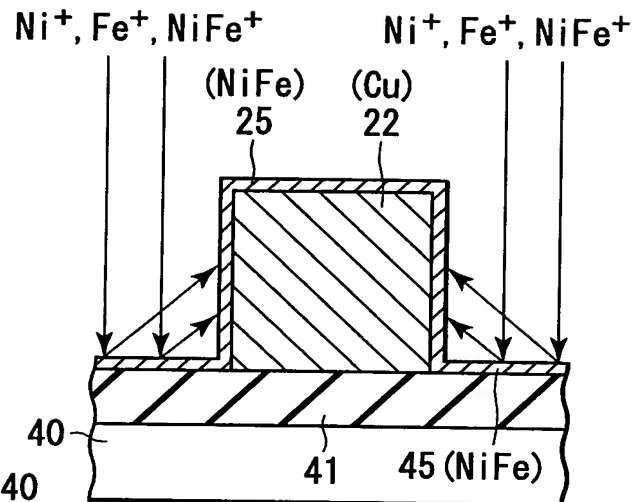


FIG. 19

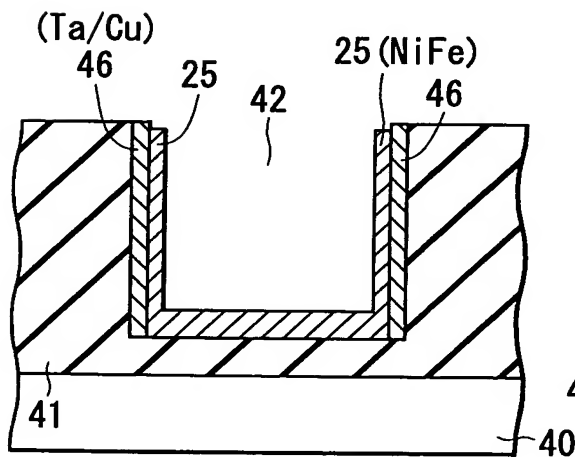


FIG. 20

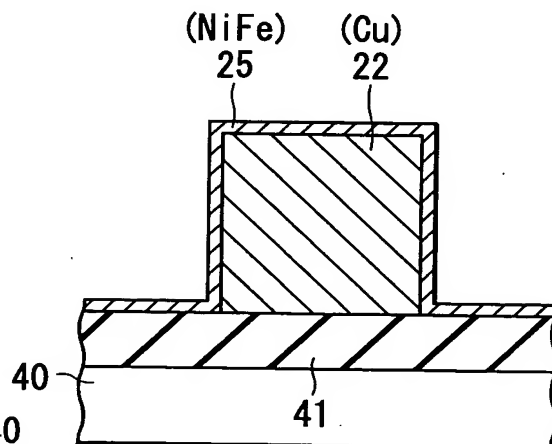


FIG. 21

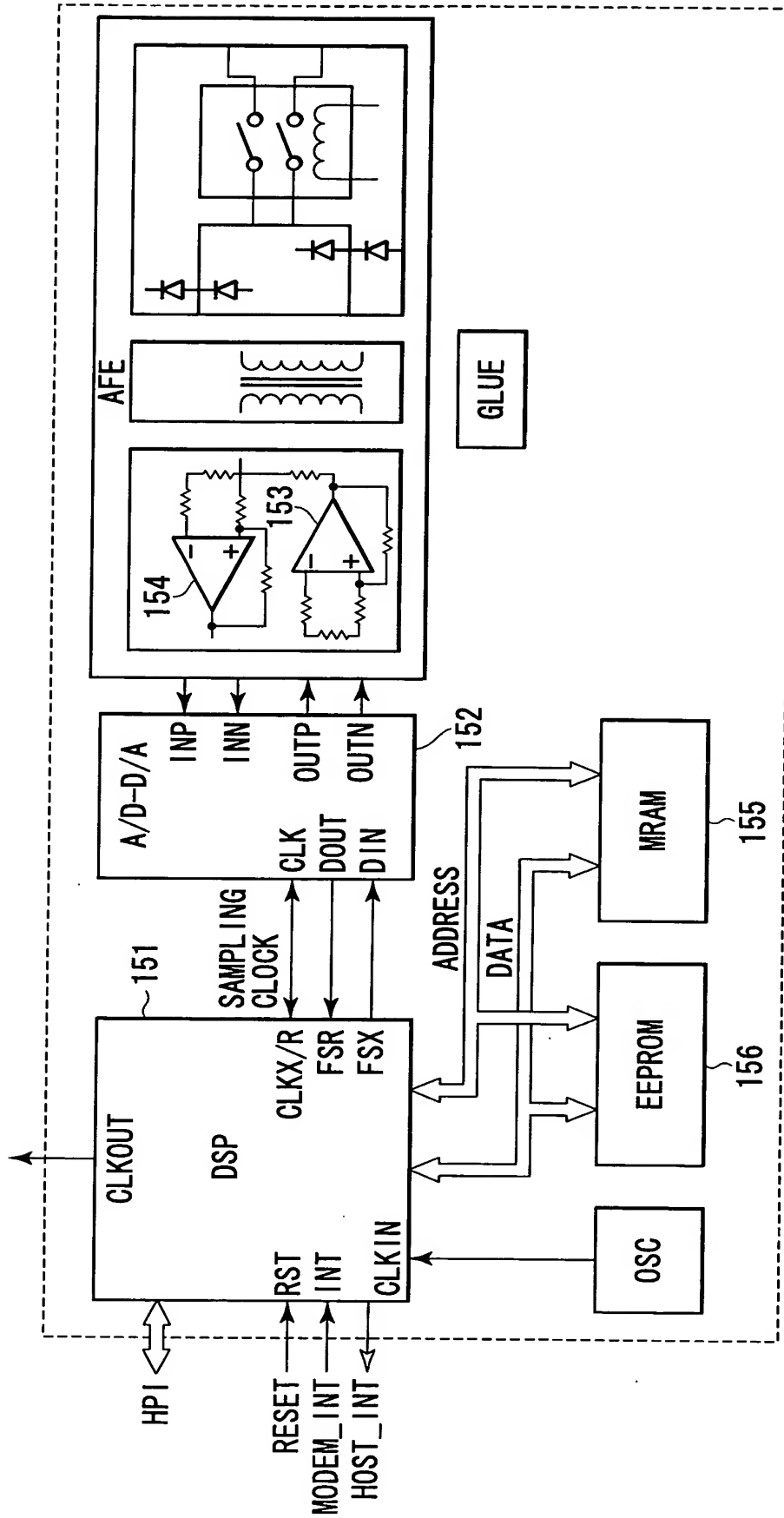


FIG. 22



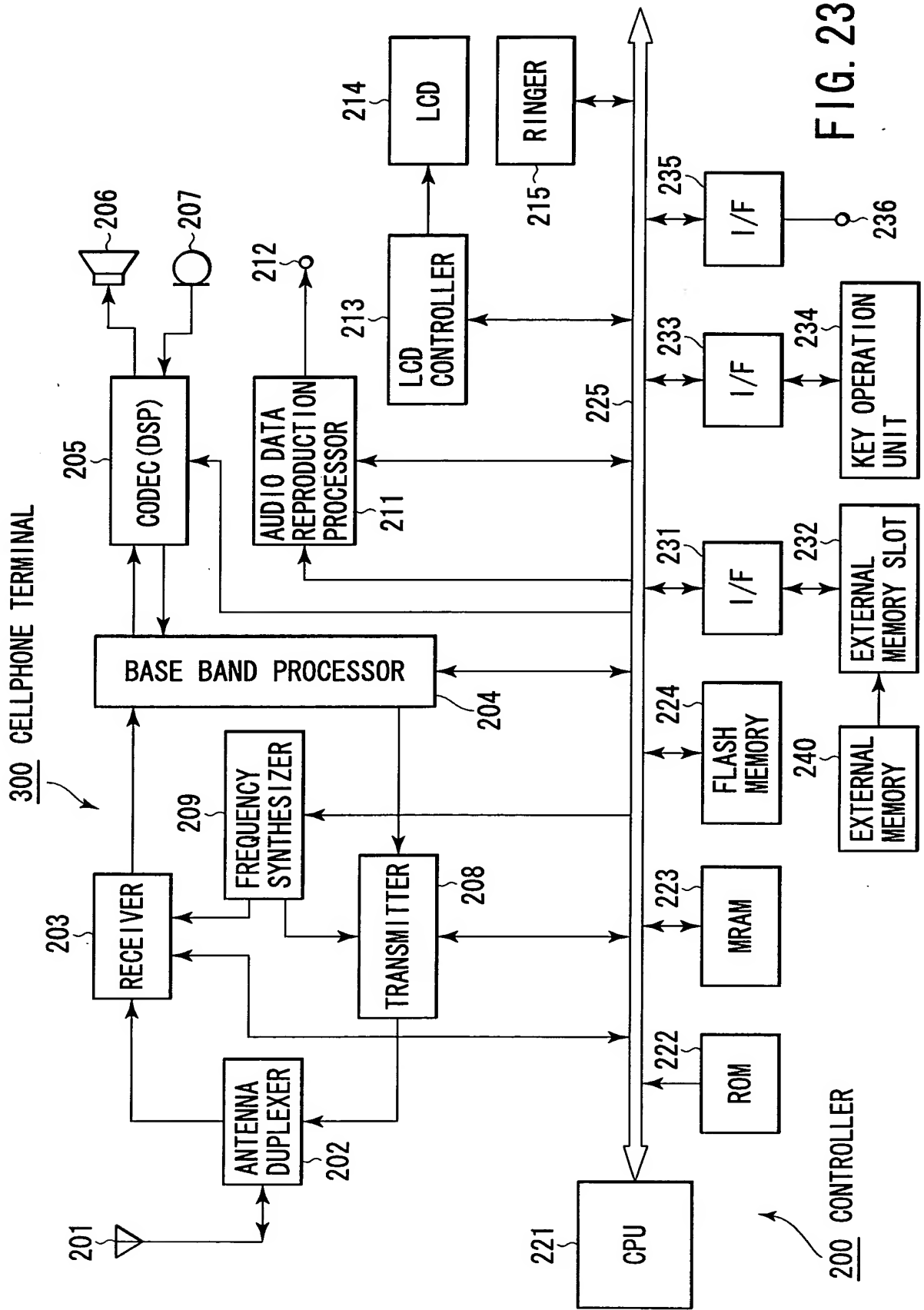


FIG. 23

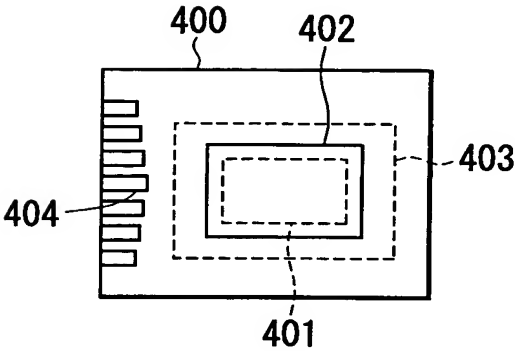


FIG. 24

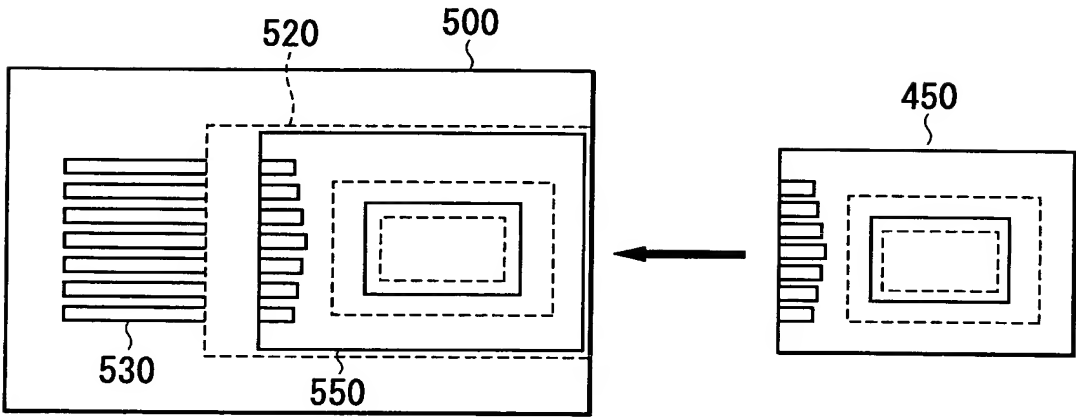
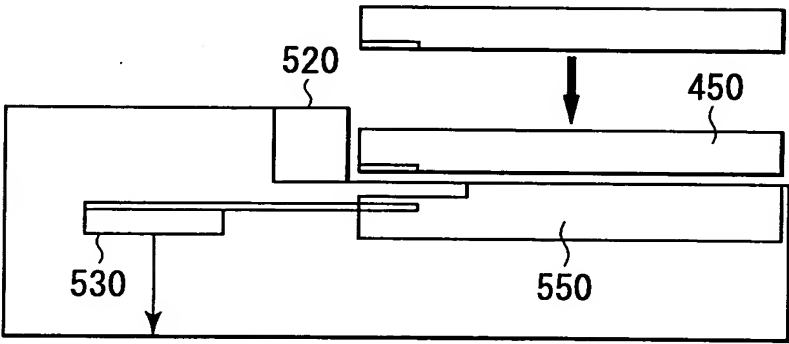


FIG. 25



TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 27

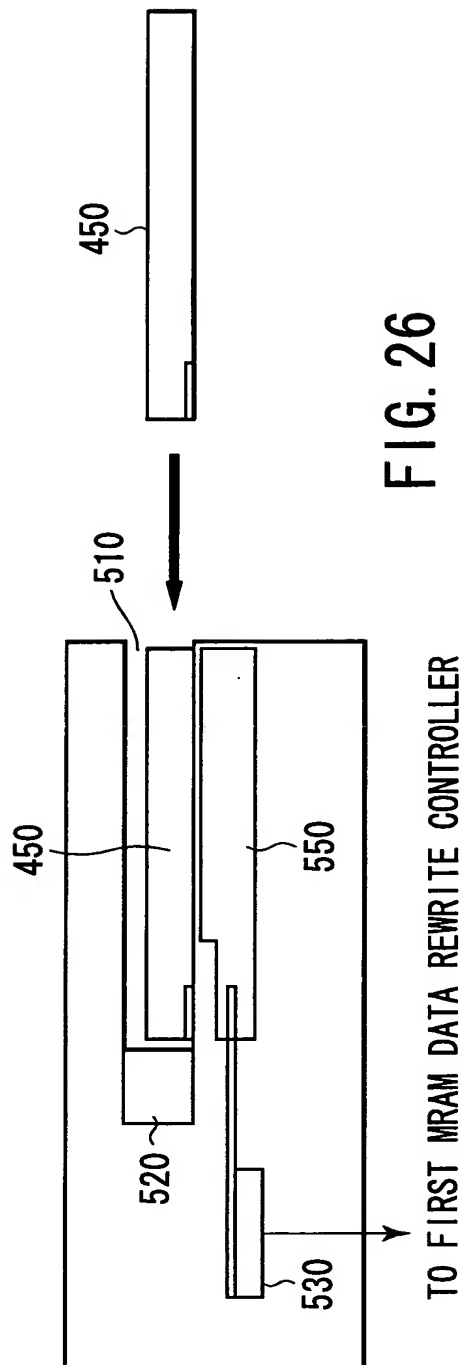


FIG. 26

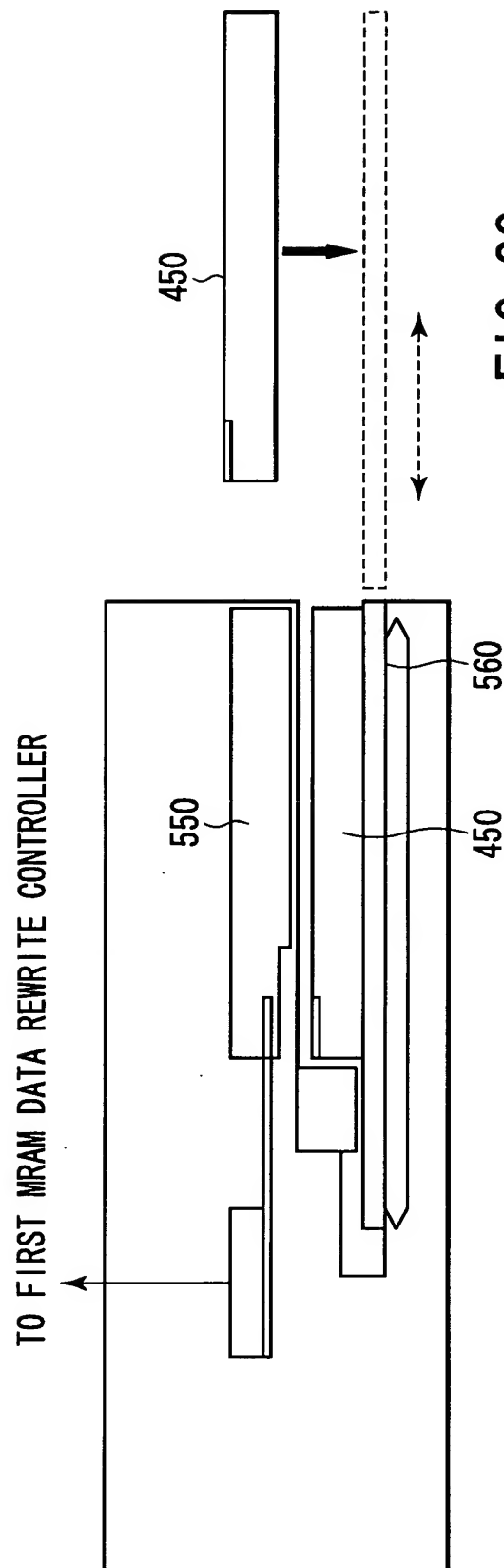


FIG. 28